=> IFW: Scan as Doc Code: SRNT <=
Doc Date:

TC 3700 Inventor Search Program

See attached inventor searches for applications and/or patents to help resolve questions of overlapping subject matter. These searches are provided as an initial examination aid: examiners should perform updated or expanded PALM or EAST inventors searches as appropriate.

Serial Number: 10/820011

1.) See attached printout of inventors listed in PALM

2.) See attached EAST Inventor Search
Printout shows Inventor search terms

PALM INTRANET

Day : Friday
Date: 7/7/2006
Time: 10:18:20

Inventor Information for 10/820011

Inventor Name	City	State/Country
YEW, CHEE KIANG	SINGAPORE	SINGAPORE
FONG, PIAU	PENANG	MALAYSIA
MATTHEW CHUA, KENG SIEW	PENANG	MALAYSIA

Appln Info | Contents | Petition Info | Atty/Agent Info | Continuity/Reexam | Foreign Data | Invento

Search Another: Application# [] Search **or Patent#** [] Search
PCT / [] / [] Search **or PG PUBS #** [] Search
Attorney Docket # [] Search
Bar Code # [] Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

US 20050033996 A1	20050210	Method and apparatus for a communication hub	713/300		Fong, Piau et al.
US 20040245674 A1	20041209	Method for packaging small size memory cards	264/272.17	425/110	Yew, Chee Kiang et al.
US 20040201969 A1	20041014	Method for packaging small size memory cards	361/737		Fong, Piau et al.
US 20040004283 A1	20040108	Direct attachment of semiconductor chip to organic substrate	257/734	257/E23.127	Yew, Chee Kiang et al.
US 20020130397 A1	20020919	DIRECT ATTACHMENT SEMICONDUCTOR CHIP TO ORGANIC SUBSTRATE	257/666	257/692; 257/727; 257/734; 257/735; 257/E23.14; 438/123; 438/411; 438/461	YEW, CHEE KIANG et al.
US 20020001882 A1	20020103	Method for adhering and sealing a silicon chip in an integrated circuit package	438/127	257/E21.502; 257/E21.505; 257/E23.079	Eng, Kian Teng et al.
US 20020000648 A1	20020103	Thin integrated circuit unit	257/678	257/E21.503; 257/E23.069; 257/E25.023	Leong, Chew Weng et al.
US 7089661 B2	20060815	Method for packaging small size memory cards	29/841	29/412; 29/417; 29/830; 29/832; 29/842; 29/855; 361/737	Fong; Piau et al.
US 7042070 B2	20060509	Direct attachment of semiconductor chip to organic substrate	257/668	257/783; 257/E23.127	Yew; Chee Kiang et al.
US 6768646 B1	20040727	High density internal ball grid array integrated circuit package	361/748	257/777; 257/E23.069; 361/767	Chen; Fung Leng et al.
US 6602803 B2	20030805	Direct attachment semiconductor chip to organic substrate	438/780	257/E23.14; 438/106; 438/455;	Yew; Chee Kiang et

				438/798	al.
US 6468831 B2	20021022	Method of fabricating thin integrated circuit units	438/108	228/180.22; 257/686; 257/724; 257/738; 257/783; 257/E21.503; 257/E23.069; 257/E25.023; 438/118; 438/125; 438/613	Leong; Chew Weng et al.
US 6387729 B2	20020514	Method for adhering and sealing a silicon chip in an integrated circuit package	438/106	257/E21.502; 257/E21.505; 257/E23.079; 438/118; 438/127	Eng; Kian Teng et al.
US 6365833 B1	20020402	Integrated circuit package	174/538	174/534; 174/557; 174/564; 257/686; 257/691; 257/738; 257/778; 257/E21.502; 257/E21.505; 257/E23.079	Eng; Kian Teng et al.
US 6278616 B1	20010821	Modifying memory device organization in high density packages	361/803	257/686; 257/E23.069; 257/E25.023; 365/230.03; 365/51; 365/63; 438/109	Gelsomini; Tito et al.
US 6274929 B1	20010814	Stacked double sided integrated circuit package	257/724	257/686; 257/700; 257/738; 257/774; 257/778; 257/E21.503; 257/E23.069; 257/E25.023	Leong; Chew Weng et al.
US 6218202 B1	20010417	Semiconductor device testing and burn-in methodology	438/15	257/48; 257/E23.039; 257/E25.023; 438/106;	Yew; Chee Kiang et al.

				438/121; 438/14; 438/25; 438/26; 438/51; 438/55; 438/64	
US 6091140 A	20000718	Thin chip-size integrated circuit package	257/691	257/730; 257/784; 257/786; 257/E23.031	Toh; Tuck Fook et al.
US 6087203 A	20000711	Method for adhering and sealing a silicon chip in an integrated circuit package	438/118	257/E21.502; 257/E21.505; 257/E23.079; 438/106; 438/119	Eng; Kian Teng et al.
US 6084306 A	20000704	Bridging method of interconnects for integrated circuit packages	257/776	257/758; 257/778; 257/E23.063; 257/E23.069	Yew; Chee Kiang et al.
US 6049129 A	20000411	Chip size integrated circuit package	257/737	257/738; 257/778; 257/784; 257/787; 257/E23.14	Yew; Chee Kiang et al.
US 5956233 A	19990921	High density single inline memory module	361/760	174/250; 174/260; 174/262; 257/685; 257/686; 257/723; 257/724; 257/777; 257/E25.011; 361/748; 361/750; 361/790	Yew; Chee Kiang et al.